Crosstalk in Multi-Channel High-Speed ADCs

Chuck Sanna, Product Marketing Engineer, Texas Instruments

In the push to increase bandwidth, range and sensitivity in wide bandwidth systems, multi-antenna and multi-sensor arrays are becoming increasingly popular. With each antenna or sensor requiring its own signal chain, many analog-to-digital converter (ADC) suppliers are integrating multiple high-speed ADCs into a single IC design. This allows hardware designers to create smaller, more power efficient multi-channel digitizers. One potential drawback to this integration is the risk of channel-to-channel crosstalk from having multiple ADC channels on a single die. Cross-talk has the potential to increase uncorrelated noise in the ADCs, reducing signal-to-noise-ratio (SNR), while coupled signals can create spurs similar to harmonic terms, reducing spurious free dynamic range (SFDR) and total harmonic distortion (THD).

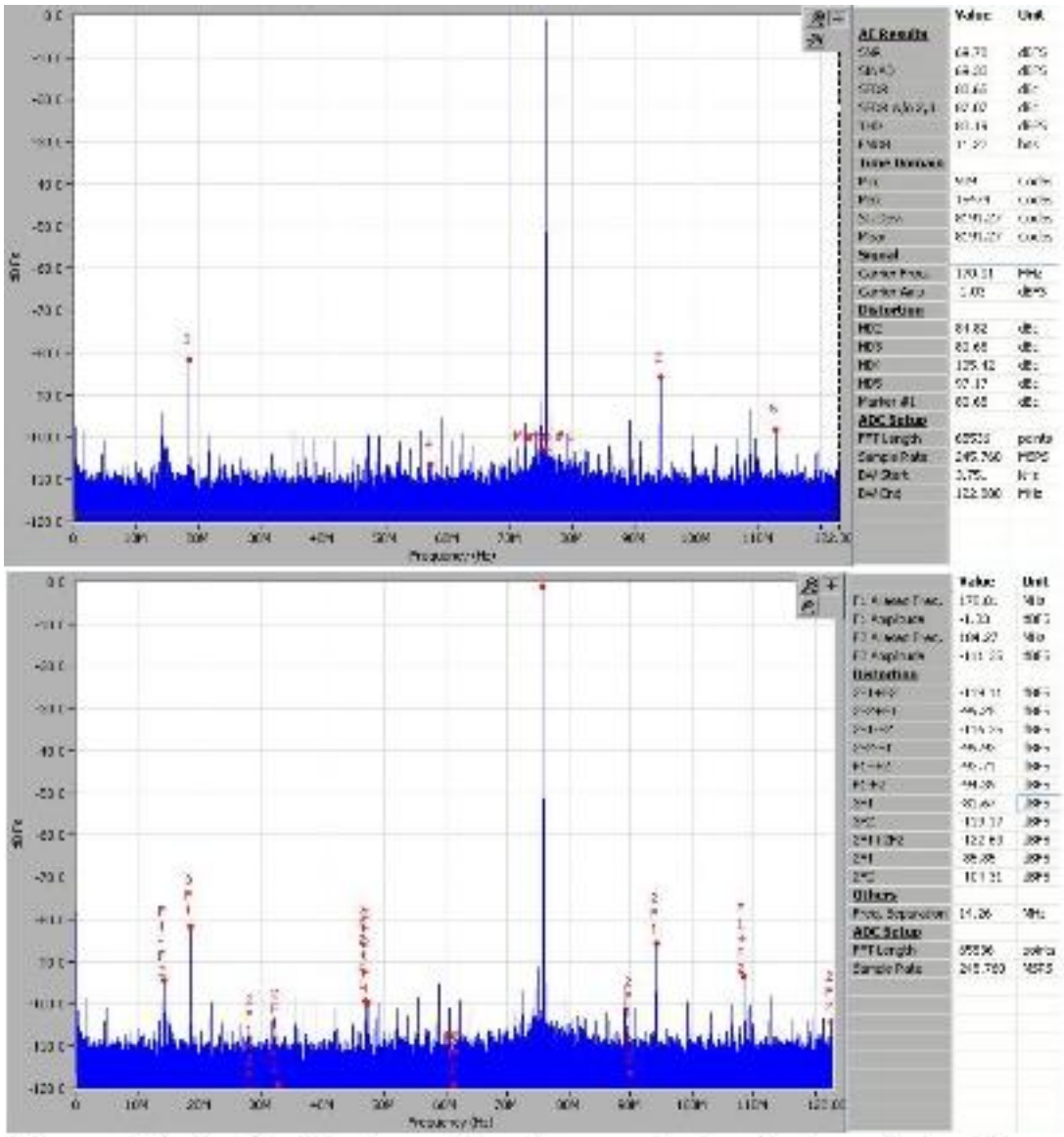
Most multi-channel ADC datasheets provide only a single, typical cross-talk number. This typical measurement is usually an idle channel measurement, where no power is input into the channel of interest and a full power tone is injected into a neighboring ‘aggressor’ channel. This may be useful to describe the basic cross-talk performance of a multi-channel ADC, but it is not indicative of real-world systems in which variable signals are expected to be input on each channel at varying strength.

Experiment Set-up

In order to create a set of measurements in the laboratory more aligned with real-world applications, an analysis is needed in which two signals of differing strength and frequency are injected into a multi-channel ADC with the outputs analyzed for noise, harmonic and mixed signal components, akin to intermodulation distortions (IMD). In order to make this analysis, a bench set-up was created around the ADS62P49, a new dual, 14-bit 250MSPS ADC from Texas Instruments, along with a companion TSW1200EVM data capture card which includes a GUI capable of analyzing noise, harmonic and IMD components. Three signal generators were used in this experiment: one to generate a clocking signal at 245.76MHz, one to generate an input frequency (IF) of 170MHz for input into the channel A port of the ADS62P49EVM, and one to generate an IF of 184.3MHz for input into channel B. Each signal was filtered by narrow-band LC filters to ensure the cleanest possible measurements, and the ADS62P49EVM is designed with wide physical separation between the input and clock circuits to minimize board-level signal coupling.

A typical output spectrum of this experiment is shown in Figure 1. In this case, a –1 dB full-scale (dBFS) signal is input into channel A at 170MHz, and a –1 dBFS signal is input into channel B at 184.3MHz. Channel A is captured in both plots, with a single-tone analysis shown in Figure 1A, and two-tone analysis shown in Figure 1B. In this set-up, the SNR of 69.7 dBFS is only slightly degraded from the data sheet typical SNR of 71dBFS at 170MHz IF, and from an SNR of 70.08dBFS captured with this EVM when channel B was idled. Of note in these figures is that the major cross-talk component appearing in the two-tone analysis is the IMD2 product. With the F1+F2

component at 92.71 dBc and F1-F2 component at 93.39 dBc, IMD2 is higher than the fourth, fifth and higher order harmonic products of the signal on channel A. Other cross-talk components, which appear with lower energy, are the second harmonic of the signal on channel B (2*F2) at 103.31 dBc and IMD3 at 98.25 dBc (2*F2+F1).



Figures 1A & 1B. Single and two-tone analysis of channel A with 170MHz, –1dBFS signal input to channel A and 184.3, –1dBFS signal input to channel B.

While the case of Figure 1 can be considered the worst-case scenario in terms of the amount of power available to be leaked from channel B into channel A combined with the amount of power in channel A to be modulated against, in a real-world situation there may be cases in which large signal amplitudes are input into the channel of interest while smaller amplitude signals are input into the aggressor channel, and vice versa. Figure 2 shows the first five harmonic components of channel A with a 170MHz, –1 dBFS input (HD2, HD3, HD4 and HD5) while the input amplitude on channel B is varied from –1 dBFS to –80dBFS. Also plotted are the cross-talk components of channel B leaking into channel A, consisting of the

channel B fundamental, second harmonic, third harmonic and intermodulation products IMD2 and IMD3.

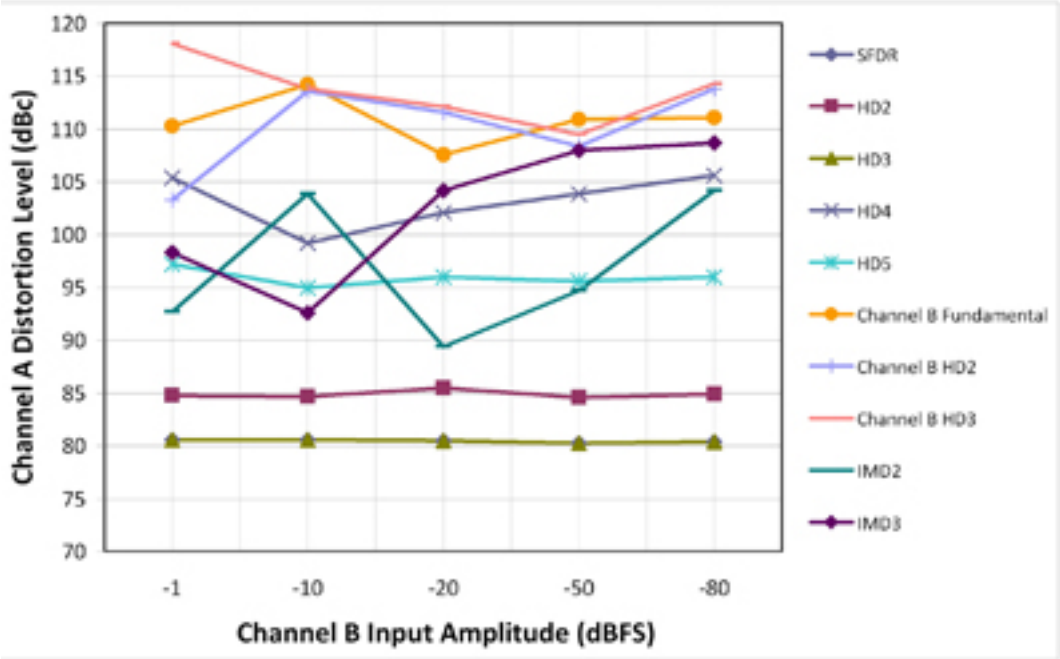


Figure 2. SFDR and cross-talk components for channel A at 245.76MSPS with 170MHz, –1 dBFS signal input to channel A and 184.3MHz signal of varying amplitude input to channel B.

Predictably, HD3 is consistently the worst spur for channel A and sets the SFDR for all cases at just over 80 dBc. HD2 is the next highest spur at around 85 dBc. However, the next highest spurious component varies with channel B amplitude. At higher input amplitudes IMD2 and IMD3 are as high as HD4 and HD5 from channel A. It is only at the lowest input amplitudes that these components are reduced below the higher order harmonic components from channel A.

Of more concern is the effect of a full-power signal input into the aggressor channel with reduced inputs on the channel of interest. Figure 3 shows the SFDR of channel A with a varying amplitude signal at 170MHz IF with a 184.3MHz, –1 dBFS signal input into channel B. This plot shows that with high input amplitudes into channel A, the IMD products are the worst cross-talk components. However, the SFDR of channel A is still determined by the harmonic components of the signal present at its own input for signals as low as –50 dBFS. It is only for signals lower than this that the cross-talk components from channel B become as high as channel A's harmonics, most notably the fundamental and second harmonic. At –80 dBFS the worst cross-talk components are 15 dB higher than the harmonic components of the input to channel A, though it should be noted that at this level these components are in the noise floor with 65,536 point data capture. Note that for input amplitudes on channel A of –10 dBFS or lower, the SNR was nearly identical if channel B was idled or if it had a –1 dBFS signal inserted.

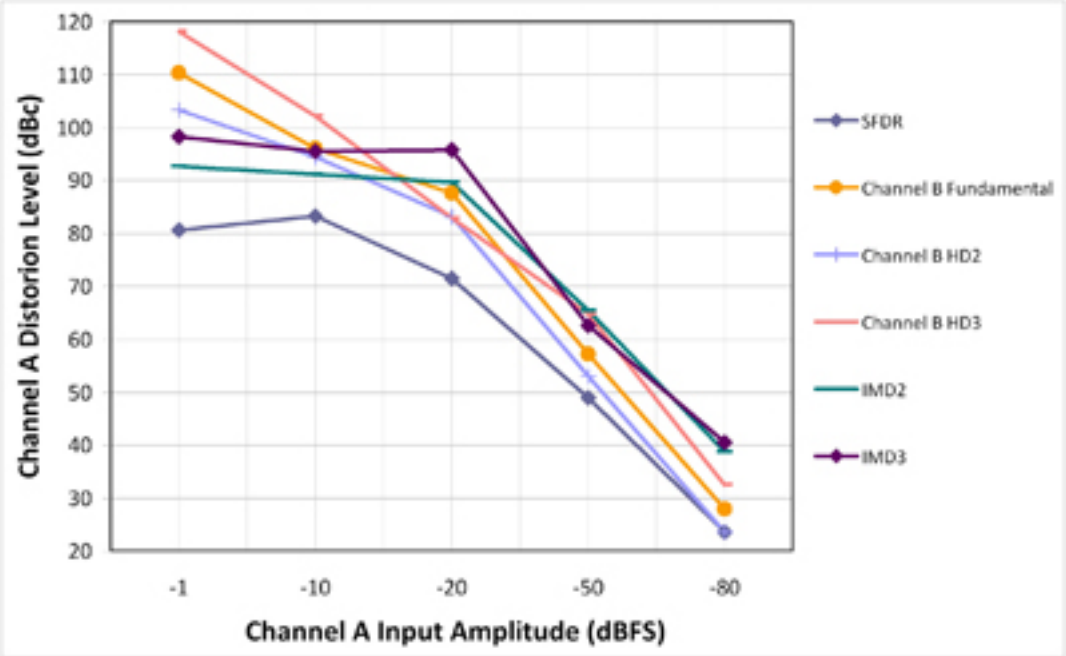


Figure 3. Single- and two-tone analysis of channel A with a varying amplitude signal at 170MHz input to channel A and a 184.3, –1 dBFS signal input to channel B.

Conclusions

Figures 2–3 demonstrate that for most situations the harmonic products of the signal incident to the channel of interest will set the SFDR. While cross-talk energy does bleed into channel A in all situations in which a signal is present on channel B, it is typically not higher than the second or third harmonic from the signal input to channel A. Except for cases where the second and third harmonics are positioned out of band through careful frequency planning, cross-talk will not be a limiting factor in systems utilizing multi-channel, high-speed ADCs. Similar experiments have been conducted on other ADCs such as the ADS6225 and ADS62P45, which utilize different core architectures, yet demonstrate results in-line with those presented here.

However, this test only demonstrates that cross-talk internal to the ADC chip is not a limiting factor for a system using a multi-channel, high-speed ADC. With differing signals being input to each channel of an ADC like the ADS62P49, great care must be taken in the circuit lay-out around the ADC. Signals can couple together at the board level in ways that can create spurious components similar to those created internal to the ADC, but at higher levels. Low-pass or band-pass anti-aliasing filters directly preceding the ADC inputs can limit harmonics generated by other components from coupling into adjacent channels, though at the cost of attenuating the signal of interest. Other common board level signal coupling that can degrade performance of both single- and multi-channel ADCs are for the clock signal to mix with an input signal, or for ripple on power supplies to couple with the input signal to create IMD spurs.

References

Download the data sheet and other technical documents for the ADS62P49 ADC: www.ti.com/ads6000-ca [1].

For more information on high-speed and precision data converters, visit: www.ti.com/dataconverters-ca [2].

About the Author

Charles (Chuck) Sanna is a product marketing engineer for high-speed ADCs and DACs at Texas Instruments, Dallas, Texas. He received a Bachelor of Science in Electrical Engineering from Northwestern University, and a Master's of Science in Electrical Engineering at the University of Texas at Dallas. Chuck can be reached at ti_chucksanna@list.ti.com [3].

Source URL (retrieved on *05/22/2013 - 11:16am*):
http://www.ecnmag.com/articles/2009/08/crosstalk-multi-channel-high-speed-adcs

Links:
[1] http://www.ti.com/ads6000-ca
[2] http://www.ti.com/dataconverters-ca
[3] mailto:ti_chucksanna@list.ti.com