Achieving High Efficiency with Power Switches

Gwan-Bon Koo, Senior Engineer, Fairchild Semiconductor

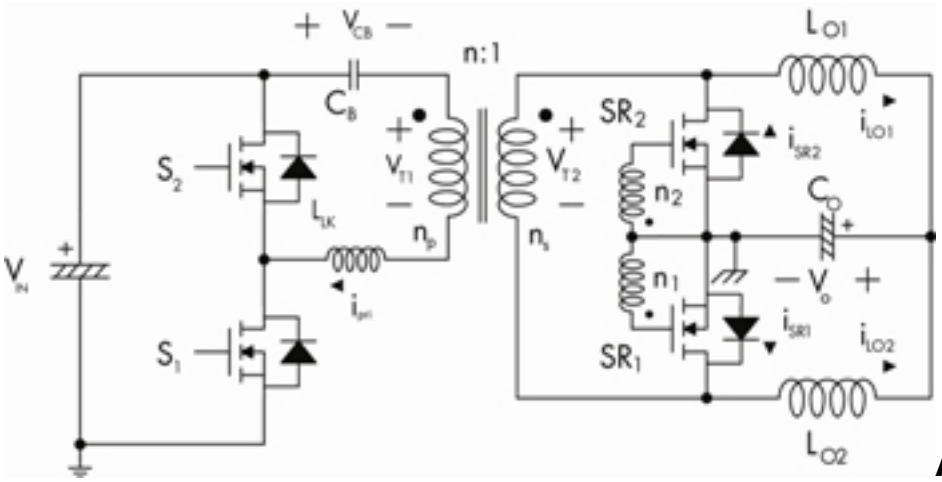
In general, high frequency operation allows the use of small-sized passive components in switch mode power supplies (SMPS), while it causes switching losses to increase in a hard switching mode. To reduce switching losses at high switching frequencies, many soft switching techniques have been developed. Among them, load resonant techniques and zero voltage transition techniques are widely used.

Load resonant techniques use a resonant feature of capacitors and inductors during whole switching period, which causes the switching frequency to be variable depending on the input voltage and load current. The change of the switching frequency, i.e., pulse frequency modulation (PFM) makes it difficult for designers to design an SMPS including input filters. Since there is no output inductor for filtering, the clamped voltage across output-rectifying diodes allows designers to select low voltage rating diodes. However, the absence of the output inductor burdens the output capacitors when the load current increases so that the load resonant techniques are not suitable for applications with high output current and low output voltage. On the other hand, the zero voltage transition techniques use a resonant feature between parasitic components during only the moment of turn-on and/or turn-off transitions in the switches. One of the advantages of these techniques is to use the parasitic components such as the leakage inductance of the main transformer and the output capacitance of the switches. So there is no need to add more external components to achieve soft switching. In addition, these techniques take pulse width modulation (PWM) up with fixed switching frequency. Therefore, these techniques are easier to understand, analyze, and design than load resonant techniques.

Due to its simple configuration and zero voltage switching (ZVS) characteristic, an asymmetric PWM half-bridge converter is one of the most popular topologies using the zero voltage transition technique. Not only that, the ripple component of the output current becomes small enough to be handled by an appropriate output capacitor due to an output inductor compared with the load resonant topologies such as LLC converters. Being easy to analyze and design and having an output

inductor, it is generally used for the applications with high output current and low output voltage e.g. PC power supplies and servers. To handle the output current more, a synchronous rectifier in the secondary side is widely used since the conduction losses can be obtained as ohmic losses instead of diode losses. It is much easier to implement the driver for the synchronous rectifier for an asymmetric PWM half-bridge converter than an LLC converter. In addition, a current doubler is a popular solution to increase the utilization of the main transformer when the output current is high.

This article describes the general features of the asymmetric PWM half-bridge converters with current doubler and synchronous rectifier. In addition, one example with some experimental results is shown using a power switch for asymmetric-controlled topologies.



Advantages of Asymmetric PWM Half-Bridge Converters with Current Doubler and Synchronous Rectifier

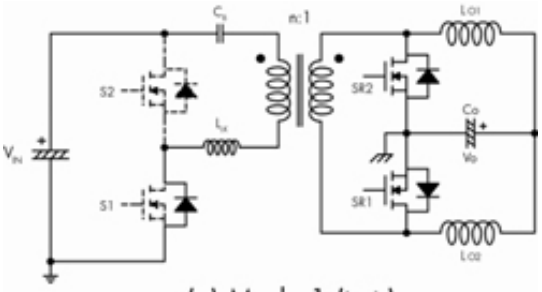
For low output voltage and high output current applications, the current doubler is widely used. Figure 1 illustrates the asymmetric PWM half-bridge converter with the current doubler on the secondary side. The secondary winding is a single-ended configuration while the output inductors are divided into two smaller inductors. To increase the total efficiency Synchronous Rectifiers (SR) comprising of MOSFETs with low RDS(ON) are used. The current doubler has several advantages compared to the conventional center-tapped configuration. First, the DC component of the magnetizing current is lower than or equal to that of the center-tapped configuration, which makes it possible for the smaller core to be used for the transformer. The amount of the magnetizing current is same as that of the center-tapped configuration when each output inductor carries half of the load current. The amount of the magnetizing current is reduced when the output inductors carry the load current unevenly.

Second, the root-mean-square (rms) value of the secondary winding current is smaller than that of the center-tapped configuration, since almost half of the load current flows through the output inductor each. Because of it, the low current density for the secondary winding could be used with the same core and the same gauge of wire. Third, the winding itself is easier than the center-tapped configuration. It is notable especially for multi-output applications because of the limitation of the pin number of the bobbin of the transformer. Fourth, the gate

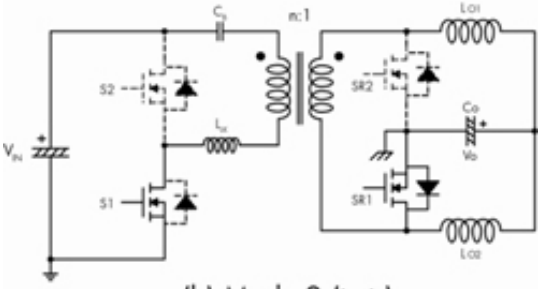
signals for SR are obtained easily and effectively from the output inductors. An appropriate gate voltage such as between 10 V and 20 V could be easily obtained from the output inductors due to the enough number of turns of them while the secondary side number of turns of the transformer is only a few. Additionally, the separated output inductors will reduce the burden of the cost of the bigger core. Because of a couple of advantages abovementioned, the current doubler is one of the most popular topologies for the high output current applications.

Operational Principles of the Proposed Converter

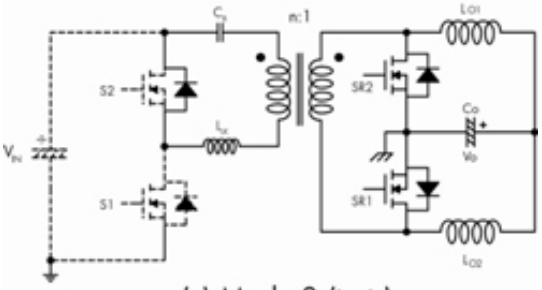
Seeing Figure 2, let’s start with Mode 2, a powering mode. Since S1 turns on, Vin-VCb is applied on the primary side of the transformer. The magnetizing current im increases with the slope of (Vin-VCb)/Lm. The



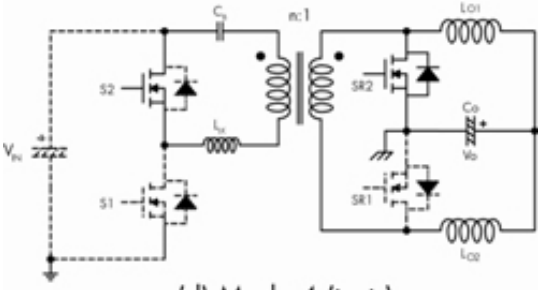
(a) Mode 1 (t_0~t_1)



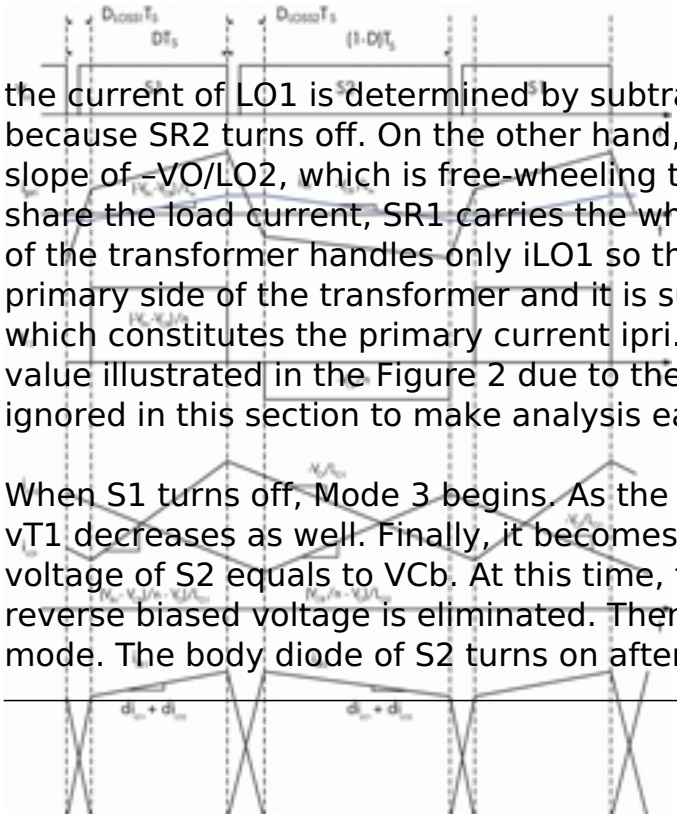
(b) Mode 2 (t_1~t_2)



(c) Mode 3 (t_2~t_3)



(d) Mode 4 (t_3~t_4)



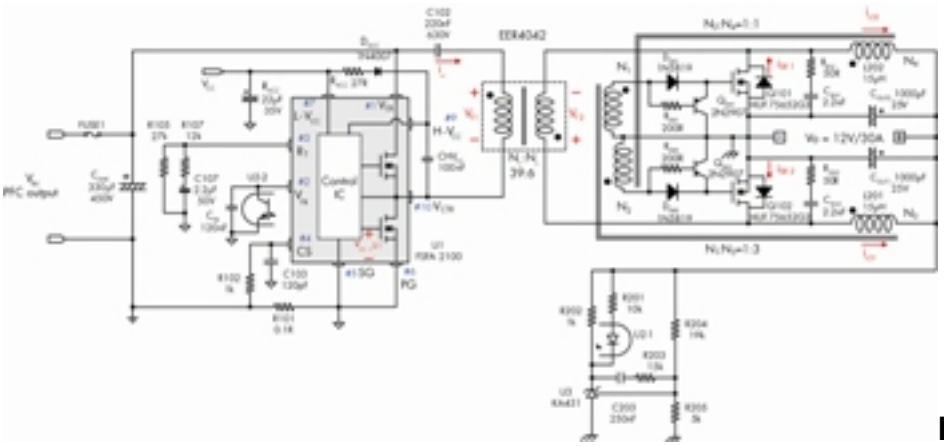
of the current of LO1 is determined by subtracting the output voltage from (Vin-VCb)/n because SR2 turns off. On the other hand, the current of LO2 decreases with the slope of –VO/LO2, which is free-wheeling through SR1. While two output inductors share the load current, SR1 carries the whole load current. The secondary winding of the transformer handles only iLO1 so that iLO1/n is the reflected current to the primary side of the transformer and it is superimposed on the magnetizing current, which constitutes the primary current ipri. In fact, vT2 is slightly lower than the value illustrated in the Figure 2 due to the leakage inductance. However, it is ignored in this section to make analysis easy.

When S1 turns off, Mode 3 begins. As the output capacitance of S2 is discharged, vT1 decreases as well. Finally, it becomes zero when the output capacitance voltage of S2 equals to VCb. At this time, the body diode of SR2 turns on since its reverse biased voltage is eliminated. Then both SRs turn on together during this mode. The body diode of S2 turns on after the output capacitance of S2 is wholly

discharged and that of S1 is entirely charged. Since both SRs turn on, iLO1 and iLO2 are free-wheeling with the slope of –VO/LO1 and –VO/LO2, respectively, and vT1 and vT2 are zero. It causes the primary current's polarity to change rapidly because VCb is applied only on the leakage inductance. When S2 turns on after the body diode of S2 conducts, the ZVS condition of S2 is achieved.

Mode 4, another powering mode starts with the end of commutation between SRs. The applied voltage on the primary side of the transformer is –VCb so that the magnetizing current decreases with the slope of –VCb/Lm and the slope of iLO2 is (VCb/n-VO)/LO2. The other inductor current is free-wheeling through SR2. As can be seen in Figure 2, the large ripple on each output inductor is cancelled because of the out-of-phase. Therefore, two smaller inductors can be used in the current doubler configurations compared with the center-tapped or bridge rectifying configurations.

When S2 turns off, Mode 1 starts as another regenerating mode. The operating principle of Mode 1 is almost same as Mode 3 except a ZVS condition. In Mode 1, vT1 becomes zero at the instant when the output capacitance voltage of S1 is equivalent to Vin-VCb. Before this instant, the load current on the output inductor LO2 is reflected to the primary side of the transformer and helps the ZVS condition of the switches to be met. On the contrary, the energy stored in the leakage inductance only has to discharge and charge the output capacitance of the switches after this instant. Therefore, the ZVS condition for S1 is harder than S2 since Vin-VCb is higher than VCb in general. Except for it, the other things can be analyzed in the same way of Mode 3. The duration of Mode 1 is obtained as



Design Example and Experimental Results

In this section, a design example will be shown. The target system is a PC power supply unit with 12 V of output voltage and 30 A of output load current as an example. Since the input comes from power factor correction (PFC) circuit in general, the range of the input voltage is not wide. The target specifications as follows:

> Nominal input voltage: 390 Vdc
> Input voltage range: 370 Vdc ~ 410 Vdc
> Output voltage: 12 V
> Output current: 30 A
> Switching frequency: 100 kHz

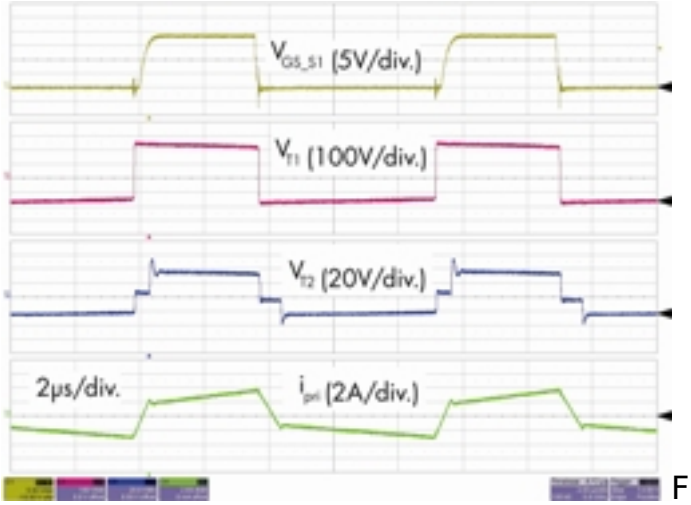
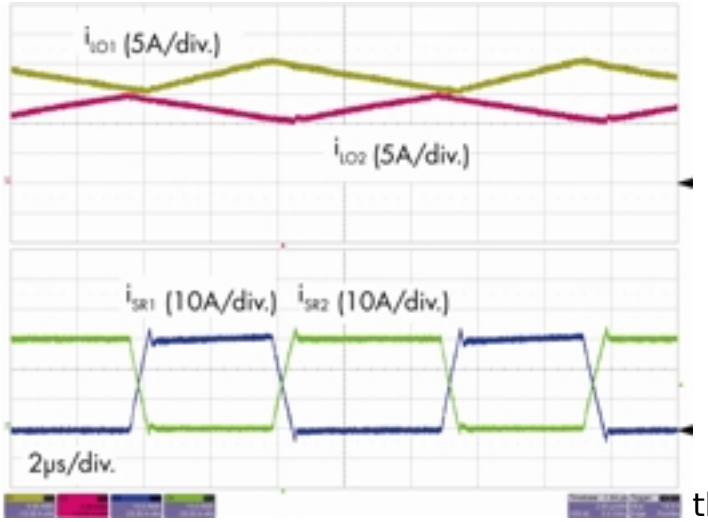
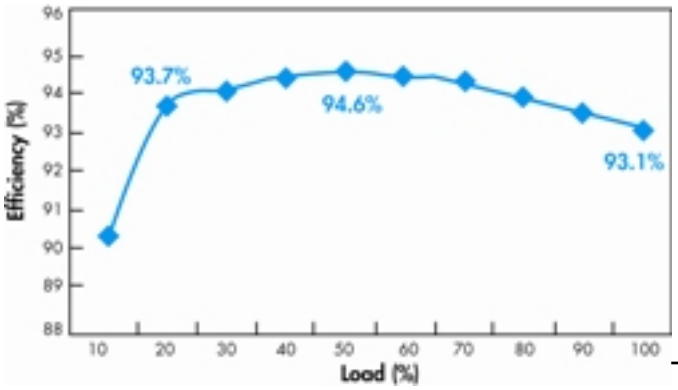


Figure 3 shows the full schematic of the reference design. The electrical features of the transformer are described in Table I.

Figures 4 and 5 show the experimental waveforms of the converter at the nominal input and the full load condition. The gate signal of S1, the primary and secondary side voltages across the main transformer and



the primary current are shown in Figure 4. It is noted that these waveforms are well agreed with the theoretical analysis including the ZVS operation. The output inductor currents and the SRs' currents are shown in Figure 5. The output inductor currents are unbalanced due to the duty ratio and the parasitic components, which mean the averaged magnetizing current is smaller than that of the center-tapped configuration.[1]



The efficiency of the converter is shown in Figure 6. The measured efficiencies are 93.7%, 94.6%, and 93.1% at 20%, 50%, and 100% of the rated load condition, respectively. It shows a marginal performance so

that the 85 PLUS program can be achieved with a well-designed PFC and dc-dc stages.

References

[1] Hong Mao, Songquan Deng, Yangyang wen, and Issa Batarseh, “Unified steady-state model and DC analysis of half-bridge DC-DC converters with current doubler rectifier,” APEC '04. Nineteenth Annual IEEE, Vol. 2, 2004, pp. 786-791
[2] Yu-Chieh Hung, Fu-San Shyu, Chih Jung Lin, and Yen-Shin Lai, “Design and implementation of symmetrical half-bridge DC-DC converter”, The Fifth International Conference on PEDS 2003. Vol. 1, Nov. 2003 pp. 338-342
[3] Panov, Y. and Jovanovic, M.M., “Design and performance evaluation of low-voltage/high-current DC/DC on-board modules,” IEEE Transactions on Power Electronics, Vol. 16, Issue 1, Jan. 2001 pp. 26-33

Source URL (retrieved on *04/25/2015 - 11:58am*):
http://www.ecnmag.com/articles/2009/02/achieving-high-efficiency-power-switches?qt-most_popular=0