Cover Story: Design Tips Cut FPGA Power Use

Design Tips Cut FPGA Power Use

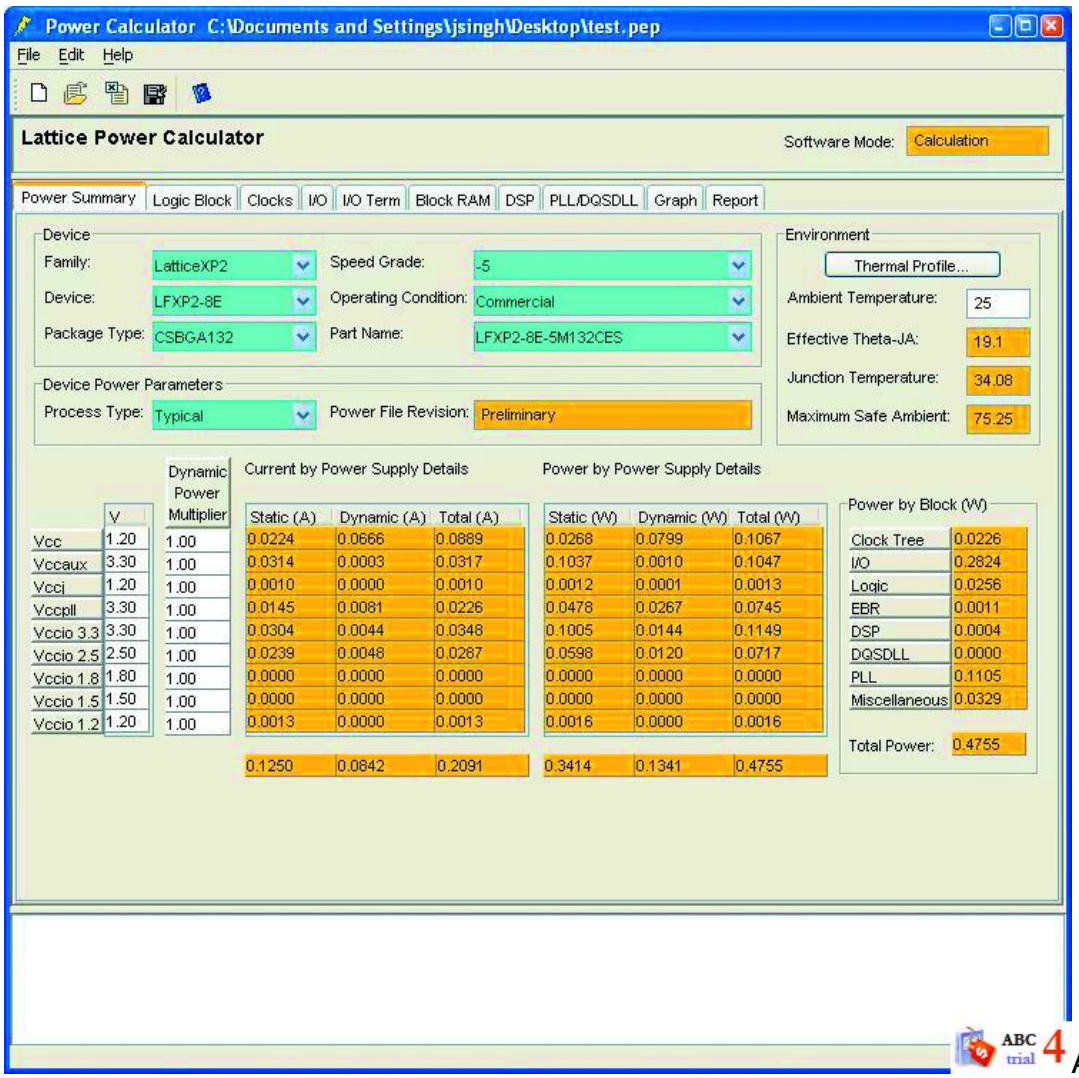
by Jon Titus, Senior Technical Editor

 Overall, the latest generations of FPGAs provide the performance engineers need for new designs. And FPGA vendors complement performance with power-saving techniques. In many cases, FPGA design tools consistently aim to implement low-power circuits, but engineers can select performance vs. power tradeoffs as well. Most of those low-power changes occur within the design tools and do not cause engineers to rework their code. But before anyone tries to reduce power, they must understand where the power gets burned. It makes no sense to reduce power consumption in an area that doesn't burn that much power to begin with.

Power divides into two classes--dynamic power and static power. The power equation $P = \frac{1}{2}CV^2f$ shows that the smaller capacitances and lower voltages of smaller-geometry FPGAs decrease *dynamic* power consumption even as clock frequencies increase. Still, engineers can use design tools to reduce dynamic power consumption. FPGA manufacturers have worked hard to also reduce *static* power consumption--the power that arises from simply powering a circuit. According to several FPGA manufacturers, static more than dynamic power has become the power you must give the most attention.

To help engineers better understand power consumption, FPGA manufacturers supply two tools, an early power-estimation tool and a post-place-and-route power-estimation tool. Typically, an early-estimation tool asks engineers to enter information, such as numbers of gates, memories, multipliers and other elements as well as types and numbers of I/O connections. They also enter information about

clock frequencies, toggle rates and so on. The tool then estimates power use based on the manufacturer's characteristics for the chosen FPGA. At this stage, engineers can approach I/O ports, memory configurations, and logic in different ways to determine how changing a design will affect power use.



After going through place-and-route steps, engineers can get a more accurate power-use report based on their implemented design. The design now includes specific clock-tree paths, device locations, signal routes, and I/O devices. A post-place-and-route power tool also can report power dissipation associated with specific clock trees, I/O devices, power rails, and logic blocks. So, engineers can look at the places where their FPGA uses the most power.

Based on their power analyses, engineers can use their design tools to make tradeoffs that reduce power and still keep performance within design specifications. As noted earlier, engineers can have FPGA design tools automatically adjust a circuit to minimize power.

The following design tips will help you save power in an FPGA design. But because FPGAs offer different capabilities, architectures and features, some of the tips below may apply to specific devices. Even in those cases, this information may prompt other power-saving ideas. These tips came from conversations with experts at FPGA manufacturers. (Please see our acknowledgments below.)

Pay attention to I/O pins. If signals will not change state often, use a pull-up or pull-down circuit that uses the least power but still maintains a pin in its proper state. Lattice, for example, provides a bus-keeper function for this purpose. Power savings may seem small until you multiply them across a 64- or 128-bit bus. When a design has unused I/O banks, if possible, don't connect their power or turn their power off.

Reduce drive voltages. If you can use a 1.2V LVCMOS interface instead of a 3.3V LVCMOS interface you save considerable power because voltage gets squared in the power equation.

In some cases, specs will dictate a bus type, but when possible, replace wide FPGA-to-FPGA buses with serialize-deserialize (serdes) connections. Some FPGAs now provide low-power multi-gigabit/sec. serdes interfaces.

Continued on next page... [1]

Links:
[1] http://www.ecnmag.com/Cover-Story-Design-Tips-Page2.aspx