

# Instruments Scope Out Bus Details

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Although serial ports may seem like antiques, for many years ahead, equipment will continue to rely on serial communications via RS-485, I2C, SPI, SATA and 10-Gigabit Ethernet links, for example. But testing and troubleshooting communications on these and other serial buses can get ugly. No one wants to sit in front of a scope to try to make sense of endless streams of 1s and 0s. “When engineers find a problem in a signal’s eye diagram, they want to ‘unfold’ the signal and examine the waveform at the point that caused the ‘eye’ violation,” said Rick Eads, senior program manager in the Digital Test Division at Agilent Technologies. “But it is difficult for standard oscilloscopes or signal-integrity instruments to zoom in on and interpret words, bytes and bits carried on that waveform.”

“The need to examine and interpret data in a bit stream starts as soon as engineers have chips to work with,” said Eric Lanning, technical lead for Finisar’s Bus Doctor products. “After engineers determine that their circuits meet signal-integrity specifications, they must ensure that those signals carry appropriate information. Thus, protocol and data analysis extend from IC testing to development, manufacturing and field service.”

## Serial Links Simplify Transfers



Serial links such as RS-485, CAN, I2C and SPI transfer bits of information in simple networks. At this level, engineers want to ensure that transmitters and receivers work, that the proper address and data information exist on the bus, and that devices respond to commands as expected. These networks have basic, if any, protocols. Bus-analysis instruments can take serial communications and express information in binary, hexadecimal and decimal forms as well as indicate the type of communication transfers. To analyze CAN-bus communications, for example, you would use an instrument that displays byte values and information such as acknowledgments, slave address and read/write conditions in an easy-to-analyze format. (Even a bus that appears simple can get complicated. The CAN bus, for example, supports high-level protocols such as DeviceNet and CANopen.)

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On the other hand, Gigabit Ethernet communications require careful attention to signal-integrity specifications as well as to proper use of complicated protocols that may have several “layers.” Those layers form a “stack” that grows from the lower physical layer, or electrical connections, to the upper application layer which can include use of the Ethernet link email, Web browser and other programs.

So, instead of looking at and interpreting low-level bits and bytes on high-end buses such as Fibre Channel, Ethernet, engineers want to view bus transactions. In a TCP/IP communication over Ethernet, a display of flags, source and destination addresses, checksum and type of service provides more information than a low-level analysis of bits.

Unfortunately, as engineers move up a protocol stack from bits to high-level messages and actions, they often employ different instruments which tend to break the continuity of test information. “They use one type of instrument to test at the physical layer and a different instrument to investigate the data-link and transaction layers,” said Randy White, serial applications engineer at Tektronix. “Without integrated instruments, engineers waste time.”

### A Variety of Instruments To Address Communications Challenges



The widespread use of serial communications — chip to chip or continent to continent — has brought forth instruments such as mixed-signal oscilloscopes, protocol analyzers and bus analyzers with capabilities that let engineers view and quickly analyze simple and complex bit streams. (In this article, I use the generic term “bus analyzer” for all these instrument functions.)

Recently, Tektronix’s White visited a company that had communication problems. “Their device worked well at the physical level, but when they connected it to a device from another vendor, the two devices would not communicate.” By using an instrument such as the Tektronix TLA7000-Series logic analyzer that combines oscilloscope and data-analysis functions, engineers could time-stamp events and then examine and correlate individual transactions to uncover the problem. “They spent two months trying to solve the problem,” said White. “With the right instrument, they found the problem in a couple of days.”

### High-Frequency Buses Ride the Learning Curve

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Engineers can face a steep learning curve when they move to a higher-frequency bus such as PCI Express, SATA or SAS, noted Dr. Michael Lauterbach, director of product management at LeCroy. “They want instruments that acquire packets of information and decode them into useful information they can relate to bus communications and external events. Then they can identify and analyze communication events and any errors or incompatibilities.” So, engineers must know a fair amount about bus operations and transactions before they jump in. Agilent’s Eads emphasized that the PCI Express (PCIe) bus takes some getting used to. When a PCIe-based computer boots up, bus negotiations establish the number of lanes and the bus bandwidth. The bus starts with a 2.5 Gbps bandwidth, but during negotiations, the computer can increase the bandwidth. “Without the capability to capture serial PCIe communications and analyze packets and their contents, engineers can run into design problems right away,” said Eads. “Also, because PCIe and many other buses use 8b/10b encoding, engineers want to look at byte values, not 10-bit waveforms.”

### The Conditions Are Right for Triggering



But, examining zillions of serial transactions broken down into bytes or high-level packets cannot help you find problems unless you know where to look. In the same way that triggers control storage-scope operations, triggers let engineers set conditions that start or stop acquisition of information in bus-analysis instruments. You can create a trigger condition to detect when a specific error condition occurs, when improper information appears in a packet, or when a certain address appears. Given an acquisition memory, or buffer, of a fixed length, you can place the trigger point almost anywhere within the buffer’s acquisition period for a given acquisition rate. Thus when the instrument detects the trigger condition, it will start to acquire information. Or, the trigger can cause the buffer to stop acquiring information. At

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times, you might set the instrument to capture data before and after it detects the trigger condition so you can see events that led to the trigger as well as conditions afterward.

“Triggering can depend on more than one condition,” noted Lauterbach of LeCroy. “In our MS-500 Mixed Signal option, you can set up voltage thresholds, bit patterns, signal edge transitions and many other conditions singly or in combinations on as many as 36 digital lines. And, you can set trigger sequences such as ‘Trigger on event X only after event Y has occurred.’ You also can acquire selective data, perhaps data associated with a specific address or with a qualifier of some sort.”

Finisar’s Bus Doctor protocol analyzer, for example, offers 12 trigger levels, each of which can have its own conditions. Think of the trigger arrangement as a small state machine. “You can set up trigger conditions where you say, ‘Look for XYZ in a command, then look for ABC in the response, and then trigger,’” explained Finisar’s Lanning. “The instrument can trigger on an event and then re-arm itself and wait for the same trigger event to occur again. Because we can capture data in 1,024 buffers, engineers could set up a test to run over a weekend and accumulate 1,024 triggered traces.”



“When you plan to buy an analyzer or mixed-signal scope, ask how its probes will affect your signals,” cautioned Lauterbach. “You don’t want an instrument to corrupt your signals and cause additional problems, but engineers may forget about interactions between probes and the signals they want to explore. In general, you want any leads from your board to a mixed-signal scope to be as short as possible.”

### **Keep the Leads From Board-To-Scope As Short As Possible**

“We recommend that engineers use a mid-bus probe when they want to analyze PCI Express signals,” said Randy White of Tektronix. “The active probe connects to PCB pads specifically placed to accept the probe in the middle of the PCI Express connection. Of course, engineers must design the ‘footprint’ on their PCB beforehand, but they might not think about the need to access PCIe signals for later testing.” Tektronix and other companies provide the mechanical and electrical

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specifications for the mid-bus probing contacts which conform to an industry standard. A removable retention module holds a mid-bus probe head against the PCB pads.

You can remove the mid-bus contacts from a PCB layout in a final board “spin” before you put the PCB into production. But White remarked that many engineers leave the pads on a board because they may want to run validation tests later on. So, if you do not need the space, leave test pads in your design.

If you do not want to, or cannot, add special probing pads, you can use an interposer board on the PCIe bus. The interposer board plugs into a vacant PCIe slot and routes the bus signals to a bus analyzer.



If a system has boards plugged into all PCIe slots, you can remove a board, insert an interposer card and plug the board into a bus socket on the interposer card. You must have some sort of standard PCIe connector available — you cannot connect here and there to PCI signal traces. Companies that sell bus analyzers also offer compatible probes and interposer cards for many buses.

Analysis of serial buses helps ensure product compatibility and tracks down errors at as high a protocol level as possible. At times, though, you may need to correlate serial-bus operations with external events. At times, you may need an instrument that provides mixed-signal capabilities and can capture, display and analyze serial and parallel information as well as digital and analog signals. Suppose you have an intelligent pressure sensor connected to a CAN bus. A mixed signal scope with bus-analysis capabilities lets you view the analog pressure signal and correlate it with CAN bus communications. Thus, you may need to think beyond the bus and ensure that your bus-analysis instrument can acquire and correlate non-bus activities and signals.

### For Further Reading

“PCI Express 2.0 Digital Validation and Debug Using Serial Logic Analysis Tools, Tektronix. September 2007. WebID: 11792.

[www2.tek.com/cmswpt/tidetails.lotr?ct=TI&cs=Application+Note&ci=11792&lc=EN](http://www2.tek.com/cmswpt/tidetails.lotr?ct=TI&cs=Application+Note&ci=11792&lc=EN)

[1]

“Protocol Analyzers vs. Logic Analyzers: Using the Right Tool for the Job,” Finisar. March 2007. [www.finisar.com/library1\\_7\\_2](http://www.finisar.com/library1_7_2) [2].

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