New Approaches Maximize Power Supply Efficiency Across All Loads

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New power regulations are redefining the meaning of efficiency in power supply design. Driven by increasing demand for electrical power worldwide, government agencies and industry groups are adopting new environmental standards that are designed to reduce power consumption by improving power efficiency. In the U.S. for example, the Department of Energy (DoE) and Environmental Protection Agency's (EPA) Energy Star program grants certification to electronics devices that meet a range of standards for power consumption. More recently, the State of California through the California Energy Commission (CEC) has implemented a mandatory program to implement more stringent power efficiency standards for external power supplies and consumer audio and video equipment sold in California.

These new standards define efficiency guidelines not only when a system is drawing maximum power, but also for consumption across the entire load range. The Energy Star program defines minimum acceptable average efficiency in active mode by measuring systems at 25 percent, 50 percent, 75 percent and 100 percent of rated load. It also requires that products meet requirements for power consumption at no-load. This latter category represents an operating condition in which many pieces of equipment spend the overwhelming portion of their time. Similarly, the CEC program dictates that consumer audio and video equipment sold in California cannot consume more than 1W of power in standby mode. A growing number of states in the U.S., as well as other countries around the globe, are looking to adopt similar standards. The scope of these regulations will inevitably be extended to include other product categories.
In many cases, by imposing strict new limits on power consumption under different load conditions, the new regulations reflect an increasing awareness of the importance of "normal" operation as opposed to theoretical maximum load conditions in reducing overall energy consumption. The recent focus on improving power efficiency at low loads makes sense. Many electronics systems and consumer appliances require relatively high power for short durations. Inkjet printers, for instance, may require up to 80W when they are driving servomotors that move print heads. Similarly, the ubiquitous external power supplies used to power and charge cordless phones, many different home appliances or power tools require relatively high loads during the charge cycle. Most of the time, however, these power supplies sit in battery maintenance mode and operate at just a few percent of their rated power.

Recent research has measured the cost of low efficiency at these low load conditions. The EPA estimates that more than three billion low voltage power supplies are being used in the U.S. to power laptop computers, printers, scanners and other devices. Worldwide, the number rises to more than 10 billion. While

individually these power supplies do not consume much in low load or standby mode, when multiplied by billions, they represent a tremendous amount of power. The state of California estimates that if 20 million external power supplies sold each year met proposed Tier 1 efficiency standards, the statewide energy savings would amount to over 96 million kWh. Nationwide, the Lawrence Livermore National Laboratory calculates that standby power costs U.S. households more the $5 billion each year.

Efficiency Without Compromise

The challenge for power supply designers is to develop circuit switching techniques that can provide good efficiency under low load conditions without sacrificing cost or compromising efficiency at high-loads. Traditionally, power supply designers have focused on maximizing power efficiency at maximum load. To accomplish this, they have typically selected PWM mode switching power supplies that offer significantly higher efficiency levels than comparable linear supplies. Switching losses limit the efficiency of these switch-mode supplies in low-power standby or sleep modes to <40 percent. To improve efficiency at lower loads, in many cases designers have opted to add a second bias power supply that allows the main power supply to turn off under low-load/no-load conditions. Relentless competition in consumer markets, however, has made the additional costs associated with a second bias supply increasingly unattractive.
Power supply designers can use a number of different strategies to meet these new regulatory requirements. One way is to boost full load efficiency. The CEC requirement places equal weight on 25 percent, 50 percent, 75 percent and 100 percent performance to determine overall efficiency. It is possible to compensate for moderate low and medium load efficiency by boosting high end performance. Simply adding a larger primary switching transistor will boost high end efficiency. The increase in performance at the high end will lead to lower moderate and low load efficiency due to increased switching losses. But the overall effect will be a small net gain in overall performance, at least in higher power systems.

Another strategy designers can use is to introduce synchronous rectification in the output stage. This approach also boosts high end performance and has a smaller impact on low end efficiency. Sophisticated regenerative snubber circuits might also help improve efficiency in these designs. A third option is to reduce the switching frequency of a PWM. This strategy might improve overall efficiency, but those gains come at the expense of larger sized magnetics and filter components as well as possible increases in audible noise. It is important to note that while these approaches allow systems to meet higher overall efficiency requirements, they inevitably add to power supply costs.

Recently, power semiconductor manufacturers have introduced a new AC/DC power conversion technology that addresses the need to improve low power efficiency without increasing cost. The new ICs continue the strategy of integrating the key power conversion elements of a flyback converter, including a switching power MOSFET, a controller and supervisory functions such as current limit, temperature limit, overvoltage and undervoltage protection into a single monolithic IC. On-board current monitoring circuitry provides the load information that allows these ICs to

react to different load conditions. A new multi-mode controller design enables power supply designers to achieve new levels of efficiency across the entire load range without the use of an additional, costly standby power supply.

One of the key advances in this new approach is the use of an innovative multi-mode control scheme which seamlessly transitions between different operating modes to optimize energy efficiency at all power levels. The power conversion IC maximizes efficiency at different loads by transitioning through four different operating modes that are designed to provide best performance under each load condition. At full load, the IC works in a high (132 KHz or 66 KHz) fixed frequency PWM mode. As load reduces, the controller moves to a variable frequency mode. At lighter loads, the converter again transitions, this time to a 30 KHz PWM mode which avoids audible noise. When the system enters low load or no-load operation, the controller again seamlessly transitions and employs a fixed peak current, multi-cycle modulation scheme to maximize efficiency. This low power mode avoids the increased audible noise and increased output ripple seen with alternative “burst mode” switching schemes. Operation in all modes and the transition between the different control schemes is completely transparent to the power supply designer who only needs to consider the high power-mode in their calculations.

Circuit Examples

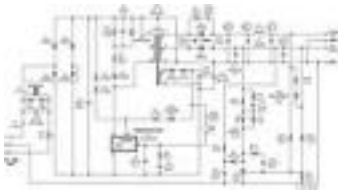

Figure 1.
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Figure 1 illustrates a universal input, 35W output, flyback power supply that uses this new technology. The circuit is applicable to a wide range of systems requiring an energy efficient dual output power supply such as an LCD monitor. AC input is rectified (D1-D4), filtered (C4) and connected across the primary side power components (T1 and U1). Components C4, L1, C7 and C11 provide EMI filtering while thermistor RT1 limits the inrush to the storage capacitors when AC is applied. Efficiency is increased so that the power supply delivers up to 35W without requiring an external heat sink.
The power supply meets CEC and Energy Star 2008 requirements by offering greater than 82 percent full load efficiency. For no-load and standby modes, the power supply offers 0.55W standby output power for 1W input. No-load power consumption is less than 300 mW at 265V AC. The power supply also meets EN55022 and CISPR-22 Class B requirements for conducted EMI with more than 10 dBµV margin.

The IC also provides a variety of safety and reliability features including overvoltage (OV) and undervoltage (UV) protection and auto-restart. Resistors R3 and R4 program the nominal UV lockout and OV shutdown limits to 103V and 450V respectively. UV lockout eliminates power-up and power-down glitches. OV shutdown protects the supply from line surges. In this design, the programmability

of the output OV function offers an extra level of design flexibility. Designers can use the Zener diode VR2 and resistor R5 to create an output OV circuit. If voltage increases at the output, it will result in increased voltage at the output of the bias winding across C10. The Zener VR2 will breakdown and current will flow into the multifunction (M) pin of IC U1. This will initiate an OV shutdown. The value of R5 is used to determine whether the shutdown is latching or non-latching.

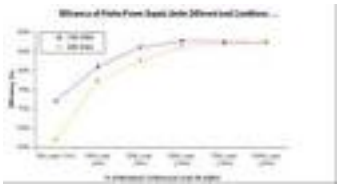
Figure 2.
(Click image to enlarge)

A second circuit is depicted in Figure 2. This isolated flyback converter supplies up to 32V output capable of delivering 20W of continuous power with an 80W peak current while operating from a universal input. A typical application for this circuit would be an inkjet printer or for an audio amplifier.
The circuit meets CEC and Energy Star requirements by delivering high efficiency in standby and sleep modes. It provides 0.6W output power for 1W input, and it enables more than 2.3W output for 3W input at 240V AC. No load input power is less than 300 mW at 240V AC. Like the previous example, the design also meets EN55022 and CISPR-22 Class B requirements for conducted EMI with more than 10 dBµV margins.

To provide a constant output power with line voltage, R11, R14 and R12 linearly reduce the internal current limit of U4 as the line voltage increases. This allows the supply to limit the output power to less than 100 VA at high line while still delivering the rated output power at low line.

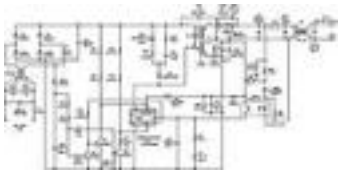
Figure 3.
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The power supply also features a time-triggered overload protection function which is sensed from the primary side bias winding. When an overload occurs, the voltage across C13 rises. Any voltage greater than 20V triggers a latching shutdown feature on the voltage monitor (V) pin. The values of C9, R20 and R22 determine the delay before triggering the OV latch. A fast AC reset circuit ensures that the V pin, once it is in latching shutdown, discharges below a fixed threshold to reinitiate switching. On loss of AC, Q3 turns off which turns on Q1 and pulls the V pin low to reset the OVP latch.

Conclusion

Given recent changes in the regulatory environment, the move to higher efficiency power supplies is inevitable. Any electronics manufacturer seeking to sell its

products in major worldwide markets must find a way to develop power supplies that offer high efficiency levels not only at full-load, but in reduced load conditions as well. By offering seamless transition across multiple switching modes, a new generation of power conversion ICs offers designers a chance for the first time to deliver excellent power efficiency at low load conditions without compromising high-end performance or increasing system cost.

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