An Introduction to RapidIO

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Years ago, designers involved with high-performance computer systems realized the parallel-bus structures found in most computers had run their course. New computer systems, such as those based on VME64x, move data across switched-fabric networks. Unlike a bus that connects all boards to all signals, a switched-fabric network routes communications through switches. Thus communications can take one of several high-speed paths and no longer create a bus bottleneck. In this context, "fabric" implies a point-to-point network that designers can "scale" to accommodate thousands of nodes. But a fabric does not imply the use of a specific hardware or software architecture.

The RapidIO approach to breaking the bus bottleneck first appeared as a standard in 1999 and was based on work underway at Motorola and Mercury Computer Systems. Although now eight years old, the standard continues to offer developers a world-class communication technology that has the support of many suppliers of integrated circuits, boards, backplanes and computer systems. Vendors of RapidIO-compatible products include Freescale Semiconductor, Lucent-Alcatel, PMC-Sierra, Texas Instruments, Tundra Semiconductor and WindRiver.

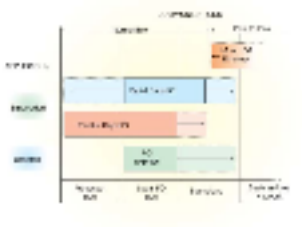
Developers can choose from more than 100 RapidIO-based products that cover a variety of development tools, embedded systems, intellectual property, software, test and measurement equipment and semiconductors (ASICs, DSPs, FPGAs, and so on). To further illustrate the interest in RapidIO, consider that nearly 55,000 embedded-system designers have downloaded the RapidIO Serial Specification and more than 1,000 have requested the key white paper, "System Interconnect Fabrics: Ethernet versus RapidIO Technology." (See: For Further Reading.)

The RapidIO standard defines three architectural layers — logical, transport and physical. The *logical layer* defines the overall protocol and packet formats; the information the end points need to initiate and complete a transaction. The *transport layer* provides the necessary route information so a packet can move from one end point to another. The *physical layer* describes circuit-level operations for packet transport, flow control, electrical characteristics and low-level error management. The layered approach prevents obsolescence, accommodates future enhancements and maintains backward compatibility with previous-generation products.

At the physical layer, RapidIO's full-duplex serial connections comply with IEEE 802.3, the 10-Gigabit Ethernet Attachment Unit Interface, usually called XAUI and pronounced "zowie." The X in XAUI stands for 10 Gbits/sec. This electrical interface operates at 1.25 GHz, 2.5 GHz or 3.125 GHz and reaches as high as 2.5 Gbits/sec after 8b/10b encoding.

The XAUI specification defines one-lane and four-lane versions. Four lanes provide

10 Gbits/sec. full-duplex communications; and the serial RapidIO (SRIO) interface can scale from 1 to 10 Gigabits/sec., which gives designers flexibility in how they apply RapidIO.



To simplify code development, The RapidIO standard provides the same programming models, addressing mechanisms and transactions for both serial and parallel implementations. Those models include basic memory mapped I/O transactions, port-based message passing and globally shared distributed memory with hardware-based coherency. RapidIO manages errors at a high level and provides means to report and recover from transmission errors. Each packet includes an end-to-end cyclic redundancy check (CRC).
To enhance interoperability, the RapidIO Trade Association has a standard functional model for semiconductor and system-design simulations to assure vendors their new boards and devices will operate with others that comply with the RapidIO specification. A RapidIO Working Group maintains and manages this open-source full-function model.

The RapidIO Trade Association has developed a set of checklists to ensure manufacturers can thoroughly test their products for compliance with the RapidIO specifications. A "gold-standard" interoperability checklist guides lab testing. Tests at a recent RapidIO Global Design Summit illustrated the value of these checklists: Components from 16 vendors worked together without fail. To ensure interoperability, vendors can use the services of RIOLAB (www.rio-lab.com [1]), an independent facility that can test device interoperability and to run the checklists.

The RapidIO specification is a single uniform protocol with limited options and consistent protocol layering; PCI is easily translated using RapidIO load/store operations which match one-to-one with PCI and PCI-e (serial PCI) operations. RapidIO has developed an encapsulation protocol to handle Ethernet packets, and designers can improve system performance when they use RapidIO to deliver Ethernet communications across a fabric. Members of the RapidIO software working groups are working on standard-use models that will solidify the complementary roles of PCI Express, RapidIO and Ethernet in next-generation systems.

The latest RapidIO specification (1.3) pulls together advanced multicast and data streaming enhancements. Specification additions will focus on demands for 5 and 6.25 Gbits/sec, channel rates and enhancements that offer carrier-grade performance. In addition, the trade association has several other enhancements under study.

For Further Reading

"System Interconnect Fabrics: Ethernet versus RapidIO Technology." RapidIO Trade Association. www.rapidio.org/outperforms_whitepaper/ [2]. Requires simple registration.

Bouvier, Dan, " RapidIO: The Interconnect Architecture for High Performance Embedded Systems,"
www.techonline.com/electronics_directory/techpaper/193101971 [3]

Fuller, Sam, "RapidIO: The Embedded System Interconnect," John Wiley & Sons, Hoboken, NJ. 2005. ISBN: 978-0-470-09291-0.

"XAUI Interface: The Components within Metro Access Networks." Xilinx. www.xilinx.com/esp/wired/optical/xlnx_net/xaui.htm [4].

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Links:
[1] http://www.rio-lab.com/
[2] http://www.rapidio.org/outperforms_whitepaper/
[3] http://www.techonline.com/electronics_directory/techpaper/193101971
[4] http://www.xilinx.com/esp/wired/optical/xlnx_net/xaui.htm
[5] mailto:Tom.Cox@RapidIO.org