

New-Generation Cartesian-Loop Transmitters for Software-Defined Radio

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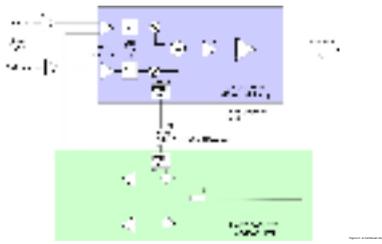
A key problem facing software-defined radio (SDR) designers occurs if the system must support linear-modulation schemes, i.e., modulations which have significant amplitude content. Such modulations present a challenge: either the power amplifier (PA) must be inherently very linear — which generally involves a very high power consumption — or some form of linearization scheme needs to be used.

The situation is complicated by another requirement often found in modern radio designs: the re-use of a solution across a range of designs. This means one solution often has to meet the requirements of hand-portables, mobiles and, in some cases, fixed stations. Further, in markets such as specialized/professional radio systems or military systems, products can span operating frequencies from 150 MHz to 1 GHz.

Various linearization schemes come to mind to meet this requirement, but the focus of this article is Cartesian feedback. With a modern integrated solution, this scheme can offer a genuine answer to all the challenges discussed above.

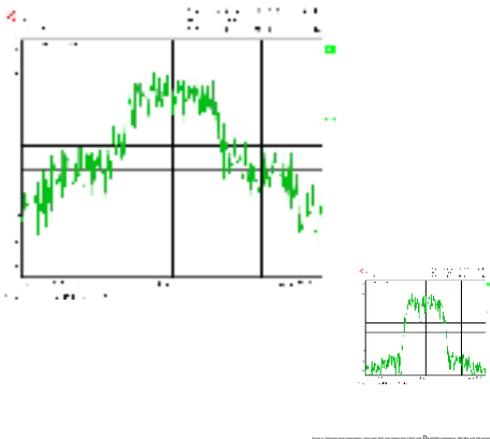
The Cartesian Feedback Loop (CFBL), first developed in the 1980s^{1,2}, is now well established as an option for highly efficient linear transmitters using modulation such as p/4-DQPSK, 8PSK and QAM. The scheme has been universally used in products implementing the TETRA standard³ and also widely used in Japanese digital technology. The loop offers a large degree of linearization improvement; gains of over 30 dB are not untypical. It is best suited to channel spacing up to approximately 200 kHz; beyond this value, designers must choose between loop stability and linearity improvement.

Integrated solutions have been in use for a number of years, but the requirements of low noise and high linearity offer a number of challenges to IC designers. Modern semiconductor processes bring performance and functionality, making the adoption of the technique over more product areas increasingly attractive and opening the door for SDR transmitters.



The loop works to improve the linearity of a PA by the action of feedback (Figure 1.) The input signal is required in in-phase and quadrature (I/Q) format. That signal is applied to a summing amplifier (or “error amplifier”), where it is compared to the feedback signal. The output of the amplifier is applied to an upconverter to generate an RF signal that is then amplified by a power amplifier.

A sample of the amplifier’s output is taken, which is downconverted and applied to the error amplifier. This closed-loop system will attempt to correct the signal at the output to match the I/Q input signal applied to the error amplifier. Figure 2 shows the effectiveness of the solution, where the upper trace is the PA operated without the feedback and the lower trace is the PA with feedback applied: in both cases, the output power is approximately the same. The closed-loop spectrum is a substantial improvement on the uncorrected performance of the PA.



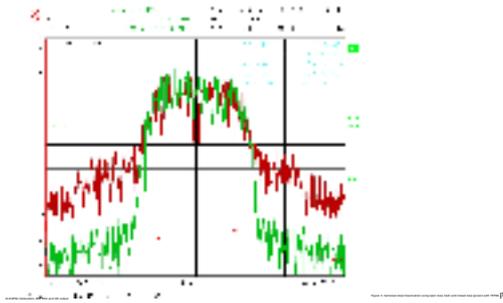
To achieve these results, it is necessary to ensure the feedback phase is correct. This can be achieved by including a variable phase shifter in the LO path. Moreover, it is necessary to include a means of constraining the loop bandwidth to ensure stability; hence a filter is included either around the error amplifier or immediately after it.

Demanding Requirements

The prerequisite for the feedback path not to introduce distortion places demanding requirements on the design in terms of linearity and noise. The need for low wideband noise also makes the design of the upconverter challenging, and the need for excellent isolation between up- and downconverter makes the Cartesian loop a testing challenge for IC designers.

Traditional markets using CFBL solutions have been 25 kHz-channeled radios at 300 MHz to 500 MHz. For some time, manufacturers have been demanding devices operating up to 1 GHz while running from 3V, taking less current than before and

not affecting performance. To examine what can be achieved with a modern CFBL design, we will use the CMX998 IC⁴ as an example.

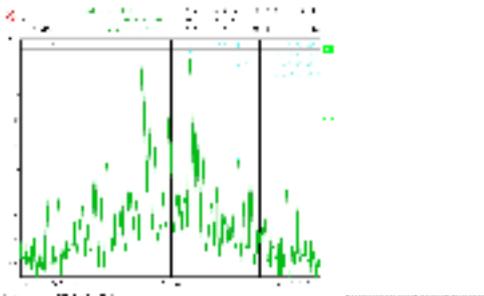


Typical Performance

The TETRA standard is a good benchmark for CFBL transmitters because it requires good linearity (-60 dBc), as shown in Figures 3 and 4.

Wideband Noise

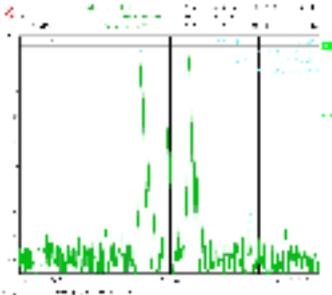
A key performance requirement for some PMR standards is low wideband noise. The Cartesian loop is like any closed-loop system in that noise inside the loop bandwidth behaves differently to noise outside the loop. Wideband noise, for example, at a 5 MHz offset, is typically outside the loop bandwidth and is generally dominated by noise from the upconverter section. Closer to the carrier, e.g. at 100 kHz, noise is generated within the loop bandwidth, and this is often dominated by the noise figure of the downconverter. The effect can be seen in Figure 5, where noise is relatively flat to approximately 500 kHz, then rolls off quickly as the edge of the loop bandwidth is reached. Also shown on the graph are the TETRA 1W and 3W requirements; it is to be observed that the CMX998-based solution easily meets these.



A Question of Versatility

Today, manufacturers are looking for versatile ICs, so that a common design can be used in multiple products. In Figure 6, operation is at 150 MHz and the output power is 10W mean, 30W peak. The Toshiba PA used in these tests is designed for FM operation (type: S-AV35), but the CMX998 produces a clean transmit spectrum, as can be seen in the lower trace on the plot. The loop being an analog system, it will reproduce whatever modulation is placed on the inputs, whether it is QPSK, GMSK, QAM, Analog FM, OFDM or others.

A tough test of the flexibility of a linearization system is a two-tone test. Although the PAPR of a two-tone signal is only 3 dB, the fact that the modulation has a zero makes it a challenge for some linearization schemes such as polar loop. In Figure 4, the Cartesian loop deals with two-tone modulation very effectively.



Future Technologies

With the trend to higher use-data requirements, there is a general move to higher on-air bit rates, which often means broader bandwidth and higher level modulations. To test performance for higher bit-rate systems, evaluation has been carried out using 16 QAM, RRC filter, $B_t = 0.2$, in a 150 kHz channel a symbol rate of 115.2 kS/s. Peak-to-average power ratio was approximately 8 dB. The measurement configuration is shown in Figure 7.

The results (Figures 8, 9) show the Cartesian feedback loop transmitter can linearize systems with 150 kHz bandwidth signals very well; approximately 25 dB linearization can be observed. One of the main alternatives to the Cartesian scheme is Polar loop. However, it is not as straightforward to implement as it appears. Typical linearization gains are relatively small (possible only 6 dB to 10 dB, compared with the 25 dB demonstrated in Figure 8 at 100 kHz offset).

References

- ¹ Petrovic, V., "Reduction of Spurious Transmitters by means of Modulation Feedback", IEE Conference on Radio Spectrum Conservation Techniques, 1983.
- ² Petrovic, V., "VHF SSB Transmitter Employing Cartesian Feedback", IEE Conference on Telecommunications, Radio and Information Technology, 1984.
- ³ ETSI EN 300 392-2 Terrestrial Trunked Radio (TETRA) voice and data. Part 2: Air Interface V2.4.2 (2004-2)
- ⁴ CMX998 Datasheet, cmlmicro.com
- ⁵ CMX981 Datasheet, cmlmicro.com

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